I. The Claims Satisfy All Formal Requirements

The Office Action rejects claims 1-20 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Office Action indicates that the term "predetermined signal" is unclear. This rejection is respectfully traversed.

The "predetermined signal" feature refers to the COM signal as shown in Fig. 3(c). Moreover, the specification discloses at page 14, lines 3-6, that "[a] signal COM corresponding to the common signal VCOM is supplied as the display signal VIN synchronously with the horizontal clock signal HCLK in a time period from the 2T period to the 3T period (hereinafter referred to as the 'common signal generation period')"; "[t]he common signal line driving circuit 400 samples the level of the signal COM supplied as the display signal VIN and outputs the sampled signal level as the common signal VCOM as shown in Fig. 3(f)"; and "[t]he common signal line driving circuit 400 functions to keep the common signal VCOM at the signal level specified by the sampled signal COM while the sample/hold driving signal SH is kept at the low level, that is, before the sample/hold driving signal SH rises to the high level."

Thus, the "predetermined signal" feature is the COM signal. The signal "SH", on the other hand, is a sample/hold driving signal, which is used for sampling and holding the signal COM included in the display signal VIN. The signal "SH" is not a "predetermined signal" included in the display signal.

Furthermore, with respect to claim 16, claim 16 recites, "a display signal generation circuit that combines the multiple pixel signals with a predetermined signal, and thereby generates one display signal." Thus, claim 16 claims that the display signal includes the predetermined signal and the multiple pixel signals. Moreover, although the display signal VIN includes a "predetermined signal", it is not equal to the "predetermined signal".

As such, it is respectfully submitted that the term "predetermined signal" is clear, and particularly points out and distinctly claims the features the Applicant regards as the invention. Accordingly, withdrawal of the rejection of claims 1-20 under 35 U.S.C. §112, second paragraph, is respectfully requested.

II. The Claims Define Patentable Subject Matter

The Office Action rejects claims 1, 2, 4-6, 8-10 and 19 under 35 U.S.C. §102(e) as being unpatentable in view of U.S. Patent No. 6,407,728 to Sekine; claims 16-18 and 20 under 35 U.S.C. §102(b) as being unpatentable in view of U.S. Patent No. 5,764,210 to Moon; and claims 3, 7 and 11-15 under 35 U.S.C. §103(a) as being unpatentable over Sekine. These rejections are respectfully traversed.

As noted above, the Interview Summary states that claims 1 and 19 defined over Sekine. Moreover, claim 17 contains the subject matter of claims 1 and 19 which was indicated as defining over Sekine during the personal interview. As such, it is respectfully submitted that claims 1, 17 and 19 define over Sekine.

Nevertheless, with respect to claims 1-15 and 17-19, as discussed in the personal interview and telephone interviews, Sekine fails to disclose an input terminal that receives a display signal including a predetermined signal used for generating a common signal and multiple pixel signals to be supplied to the multiple pixels, the predetermined signal is embedded into a predetermined period between a group of pixel signals and another group of pixel signals in the display signal, as recited in claim 1, and similarly recited in claims 17 and 19.

Instead, Sekine discloses the sample hold circuit 111 is provided for sampling and holding image signals for one horizontal time period (col. 9, lines 63-65; Fig. 3). To be more specific, the sample hold circuit 111 samples and holds multiple pixel signals included in a display signal for one horizontal time period, one by one, and the multiple pixel signals are

then output separately from respective output terminals of the sample hold circuit 111. Thus, for a certain horizontal time period, each of the different pixel signals is output from each of the output terminals of the sample hold circuit 111. Because of this arrangement, with respect to plural horizontal time periods, as shown by D1 in Fig. 4, one pixel signal is sequentially output per one horizontal time period (Th period) from each of the output terminals of the sample hold circuit 111.

Moreover, Sekine discloses that in the first half period "Tdat" of one horizontal time period (Th period), each of the first switches 112 switches to connect the fixing terminal and the output terminal of the sample hold circuit 111 (the second switching terminal "B"), and in the second half period "Tcom", each of the first switches 112 switches to connect the fixing terminal to a single panel-common line "Com" (the first switching terminal "A") (col. 11, line 66 - col. 12, line 24; Fig. 3). As shown by C1 in Fig. 4, a common voltage signal is applied to the single panel-common line "Com" (Fig. 4). With respect to a certain horizontal time period, the fixing terminal of the first switches 112 outputs a pixel signal to amplifiers 113 in the first half period "Tdat", and in the second half period "Tcom", a common voltage signal is output to the amplifiers 113. As such, with respect to a plurality of horizontal time periods, a pixel signal and a common voltage signal are alternately input to the amplifiers 113 from the fixing terminal of the switches 112. Thus, a common voltage signal is put between a pixel signal and another pixel signal.

For the Examiner's convenience, a drawing figure (Fig.) is attached illustrating the differences between Sekine and claims 1, 17 and 19. In Sekine, a pixel signal D1 and a common voltage signal COM are alternately input to the amplifiers 113 as shown in (C) of the figure. In the above case, a common voltage signal COM is put between a pixel signal D1 and another pixel signal D1. As shown in (D), a pixel signal D2 and a common voltage signals COM are alternately input to the amplifiers on the right side of the amplifiers 113. In

the above case, a common voltage signal COM is put between a pixel signal D2 and another pixel signal D2. As shown in (E), a pixel signal D3 and a common voltage signal COM are alternately input to the amplifiers on the right side of the above amplifiers. In the above case, a common voltage signal COM is put between a pixel signal D3 and another pixel signal D3.

However, Sekine cannot provide all of the features of claims 1, 17, or 19. For example, Sekine cannot generate the signals shown in (A) of the attached drawing figure. In (A) of the figure, a predetermined signal COM for generating a common signal, which is included in a display signal VIN that is input to an input terminal of a liquid crystal device, is embedded between a group of pixel signals D1, D2, ... , Dn and another group of pixel signals D1, D2, ... , Dn.

Thus, Sekine fails to disclose all of the features of claims 1, 17 and 19. As such, it is respectfully submitted, that claims 1, 17 and 19 are distinguishable over the applied art. Furthermore, claims 2-15, which depend from claim 1, and claim 18, which depends from claim 17, are likewise distinguishable over the applied art for at least the reasons discussed above, as well as for additional features they recite. Accordingly, withdrawal of the rejections under §§102 and 103 is respectfully requested.

With respect to the rejection of claims 16-18 and 20, Moon fails to disclose a display signal generation circuit that combines the multiple pixel signals with a predetermined signal, which is used for generating a common signal to be commonly supplied to the multiple pixels, as claimed in claims 16 and 17; or combining the multiple pixel signals with a predetermined signal, which is used for generating a common signal to be commonly supplied to the multiple pixels, and thereby generating one display signal, as claimed in claim 20.

Instead, Moon discloses that a video signal input to common electrode correcting circuit 15 is integrated by integrator 17 and held by sampling/holding portion 18; that gain controller 19 controls the voltage of the data waveform of sampling/holding portion 18, and